MORRIS, NICHOLS, ARSHT & TUNNELL LLP

1201 NORTH MARKET STREET
P.O. BOX 1347
WILMINGTON, DELAWARE 19899-1347

302 658 9200
302 658 3989 FAX

JEREMY A. TIGAN
302 351-9106
jtigan@morrisnichols.com

July 16, 2021

VIA E-FILING

The Honorable Richard G. Andrews
United States District Court
for the District of Delaware
J. Caleb Boggs Federal Building
844 N. King Street
Wilmington, DE 19801

Re: ***XMTT, Inc. v. Intel Corporation***
C.A. No. 18-1810-RGA

Dear Judge Andrews:

In its recent Scheduling Order, and at XMTT's request, the Court adopted a supplemental claim construction schedule that provided XMTT an opportunity to propose applying the constructions in the Patent Trial & Appeal Board's Final Written Decision to this case. *See* D.I. 170 at 2-3. XMTT declined to take that opportunity (it chose not to file an opening letter due last Friday), conceding that the terms at issue are governed by plain and ordinary meaning. Accordingly, Intel respectfully requests that the Court apply the plain meaning in this litigation and reject the Board's deviation from that plain meaning. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) ("the words of a claim 'are generally given their ordinary and customary meaning'") (quotation omitted).

During the IPR, the Board addressed the meaning of two limitations which neither party sought to construe, either in the District Court or at the PTAB—the "serial processor" and "parallel processors" limitations of the asserted patents.[1] The processors are defined as components in the claimed system, as the plain language of claim 1 of the '388 patent (excerpted below) shows:

[1] Although only the '388 Patent was at issue in the IPR, the '879 Patent includes claim language similar to the "serial processor" and "parallel processor" limitations on which the Board's Final Written Decision focused. *See*, *e.g.*, '879 Patent, claim 1 ("a serial processor to execute instructions in a computing program primarily in serial").

> **1**. An apparatus comprising:
> a serial processor adapted to execute software instructions in a software program primarily in serial;
> a serial memory adapted to store data for use by the serial processor in executing the software instructions primarily in serial;
> a plurality of parallel processors adapted to execute software instructions in the software program primarily in parallel; and
> ***

However, late in the IPR—at the oral hearing—the Board raised the question of whether those "processors" should be defined based on the operation of individual components or the operation of "the system as a whole" and concluded it was the latter, even though that interpretation admittedly differed from that of either party. *See* Ex. A, Final Written Decision, at 9. The Board's analysis was based on two additional terms recited in separate limitations of some claims, a "serial processing mode" and "parallel processing mode." that refer to the "system as a whole." *Id.* at 10-11. The Board concluded that those terms refer to "the system as a whole" and, based on those terms, decided that the "serial processor" and "parallel processor" terms must also be defined by the operation of the system as a whole—effectively conflating distinct limitations of the claims. *See id.* at 11-12.

Following the issuance of the Scheduling Order, the parties conferred to determine whether and how XMTT proposed applying the Board's constructions in this case. At first, XMTT contended that this Court should take a similar path to the Board and adopt constructions—further modified by XMTT—that also conflated the "processor" terms with the "mode" terms. *See, e.g.*, Ex. B, Correspondence between XMTT and Intel, at 4-5 (construing the "serial processor" to be a "processor adapted to execute software instructions in a software program in a serial processing mode (i.e., a mode where the apparatus executes primarily in serial on the serial processor)"). Intel, by contrast, contended that the claims should be read according to their plain meaning—as the parties had done throughout discovery and claim construction. *See id.* at 3-4. A half-hour before its opening letter was due, however, XMTT changed positions and stated that it had "decided to proceed under the plain and ordinary meaning of the claim terms" and waived its opportunity to raise any dispute. *See id.* at 2.

In light of XMTT's last minute change of position, Intel followed up to confirm that the parties had a shared understanding of the plain and ordinary meaning—that the "processor" limitations describe the configuration of individual processors, not the system as a whole:

> Thank you for the update. We would like to confirm that we are in agreement regarding the plain meaning of the relevant aspect of the claims. By Intel's understanding, the plain meaning of the "serial processor" and "plurality of parallel processors" limitations (listed in full below) describes the configuration of individual processors, not the system as a whole. In other words, the claimed system must include a distinct "serial processor" adapted to execute instructions primarily in serial and distinct "parallel processors" adapted to execute instructions primarily in parallel, regardless of whether the system has or is operating in a "serial processing mode" or a "parallel processing mode." The "serial processing mode" and "parallel processing mode" are separate limitations. Please confirm XMTT's agreement or let us know if there is a dispute.

Ex. B at 2. XMTT has not offered a different understanding, nor has XMTT disagreed with Intel's articulation of the plain and ordinary meaning. *See id.* at 1. Accordingly, there is no dispute that the plain meaning, not the Board's construction, governs the "serial processor" and "parallel processor" limitations.

Intel therefore respectfully requests that the Court adopt the plain and ordinary meaning for the "serial processor" and "parallel processors" limitations and clarify that the Board's departure from the plain meaning does not apply in this litigation. *See Phillips*, 415 F.3d at 1312. A proposed claim construction order is attached.

Respectfully,

/s/ Jeremy A. Tigan

Jeremy A. Tigan (#5239)

JAT:lo
Attachments
cc: Clerk of the Court (*via CM/ECF*)
All Counsel of Record (*via CM/ECF and email*)

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

XMTT, INC.,	)	
	)	
Plaintiff,	)	
	)	
v.	)	C.A. No. 18-1810 (RGA)
	)	
INTEL CORPORATION,	)	
	)	
Defendant.	)	

[PROPOSED] CLAIM CONSTRUCTION ORDER

The Court, having considered the Final Written Decision issued by the Patent Trial and Appeal Board in *Intel Corporation v. XMTT, Inc.*, IPR2020-00145, **HEREBY ORDERS** that the terms of U.S. Patent Nos. 7,707,388 ("the '388 patent") and 8,145,879 ("the '879 patent") set forth in the chart below are construed to have their plain and ordinary meaning.

The Court further determines that the plain and ordinary meaning of the "serial processor" and "plurality of parallel processors" limitations (listed in full below) describes the configuration of individual processors, not the system as a whole. The claims require a distinct "serial processor" adapted to execute instructions primarily in serial and distinct "parallel processors" adapted to execute instructions primarily in parallel, regardless of whether the system has or is operating in a "serial processing mode" or a "parallel processing mode."

Claim Term	Court's Construction
"a serial processor adapted to execute software instructions in a software program primarily in serial" "a serial processor coupled to the broadcast network and adapted to execute software instructions in a software program primarily in serial" <u>Claims:</u>	Plain and ordinary meaning: The plain meaning describes the configuration of an individual processor, not the system as a whole. In other words, the claimed system must include a distinct "serial processor" adapted to execute instructions primarily in serial, regardless of whether the system has or is operating in a "serial processing mode." The "serial processing mode" is a separate limitation.

Claim Term	Court's Construction
'388 Patent – Claims 1, 19, 32	
"a serial processor to execute instructions in a computing program primarily in serial" Claims: '879 Patent – Claims 1, 20	Plain and ordinary meaning: The plain meaning describes the configuration of an individual processor, not the system as a whole. In other words, the claimed system must include a distinct "serial processor" to execute instructions primarily in serial, regardless of whether the system has or is operating in a "serial processing mode." The "serial processing mode" is a separate limitation.
"a plurality of parallel processors adapted to execute software instructions in the software program primarily in parallel" "a plurality of parallel processors coupled to the interconnection network and adapted to execute software instructions in the software program substantially in parallel" Claims: '388 Patent – Claims 1, 19, 32	Plain and ordinary meaning: The plain meaning describes the configuration of individual processors, not the system as a whole. In other words, the claimed system must include distinct "parallel processors" adapted to execute instructions primarily in parallel, regardless of whether the system has or is operating in a "parallel processing mode." The "parallel processing mode" is a separate limitation.
"a plurality of parallel processors to execute instructions in the computing program primarily in parallel" Claims: '879 Patent – Claims 1, 20	Plain and ordinary meaning: The plain meaning describes the configuration of individual processors, not the system as a whole. In other words, the claimed system must include distinct "parallel processors" to execute instructions primarily in parallel, regardless of whether the system has or is operating in a "parallel processing mode." The "parallel processing mode" is a separate limitation.

SO ORDERED this __ day of July, 2021.

Richard G. Andrews
United States District Judge